

AMENDMENTS TO THE CLAIMS

Please amend claims 18 and 19 as set forth below:

1 1. (original) A content addressable memory (CAM) device comprising:
2 first and second rows of CAM cells;
3 a first pair of match lines coupled to the first row of CAM cells;
4 a second pair of match lines coupled to the second row of CAM cells; and
5 a first logic circuit coupled to a first match line of the first pair of match lines and to
6 a first match line of the second pair of match lines, the first logic circuit being
7 configured to output a match signal in a first state if both the first match lines
8 indicate a match condition, and to output the match signal in a second state if
9 either of the first match lines indicates a mismatch condition.

1 2. (original) The CAM device of claim 1 further comprising:
2 a first priority encoder coupled to the first match line of the first pair of match lines
3 and to the second match line of the second pair of match lines; and
4 a second priority encoder coupled to the second match line of the first pair of match
5 lines and to the first match line of the second pair of match lines.

1 3. (original)The CAM device of claim 2 wherein the first priority encoder is also
2 coupled to receive the match signal output from the first logic circuit.

1 4. (original) The CAM device of claim 1 further comprising a select circuit to output
2 either a match signal present on the first match line of the first pair of match lines or
3 the match signal output from the first logic circuit, depending on the state of a first
4 select signal.

- 1 5. (original) The CAM device of claim 4 further comprising:
2 an interface to receive an instruction; and
3 an control circuit coupled to receive the instruction from the interface and
4 configured to output the first select signal in either a first logic state or a
5 second logic state according to the instruction.
- 1 6. (original) The CAM device of claim 5 wherein the control circuit is configured to
2 generate the first select signal in a first state if the instruction indicates a single-
3 word compare operation and in a second state if the compare instruction indicates a
4 multiple-word comparand compare operation.
- 1 7. (original) The CAM device of claim 4 further comprising a configuration circuit to
2 store a mode value and configured to output the first select signal in either a first
3 logic state or a second logic state according to the mode value.
- 1 8. (original) The CAM device of claim 1 wherein each of the CAM cells within the
2 first row of CAM cells comprises:
3 a storage circuit; and
4 first and second compare circuits coupled to the storage circuit.
- 1 9. (original) The CAM device of claim 8 wherein the first match line of the first pair
2 of match lines is coupled to the first compare circuit of each of the CAM cells
3 within the first row of CAM cells, and wherein the second match line of the first
4 pair of match lines is coupled to the second compare circuit of each of the CAM
5 cells within the first row of CAM cells.

- 1 10. (original) The CAM device of claim 1 further comprising a second logic circuit
2 coupled to the second match line of the first pair of match lines and to the second
3 match line of the second pair of match lines, the second logic circuit being
4 configured to output a match signal in the first state if both the second match lines
5 indicate a match condition, and to output the match signal in the second state if
6 either of the second match lines indicates a mismatch condition.
- 1 11. (original) The CAM device of claim 10 further comprising a select circuit coupled
2 to receive the match signal generated by the first logic circuit and the match signal
3 generated by the second logic circuit, the select circuit being responsive to a select
4 signal to output either the match signal generated by the first logic circuit or the
5 match signal generated by the second logic circuit.
- 1 12. (original) The CAM device of claim 11 further comprising a configuration circuit
2 to store a mode value and to output the select signal in either a first logic state or a
3 second logic state according to the mode value.
- 1 13. (original) The CAM device of claim 11 further comprising:
2 an interface to receive a compare instruction; and
3 a control circuit coupled to receive the instruction from the interface and configured
4 to output the select signal in either a first logic state or a second logic state
5 according to the compare instruction.
- 1 14. (original) The CAM device of claim 1 further comprising a storage circuit coupled
2 to the first match line of the first pair of match lines to store a match value

3 indicative of the state of the first match line of the first pair of match lines.

1 15. (original) The CAM device of claim 14 further comprising a logic AND gate
2 coupled to receive the match value from the storage circuit and coupled to the first
3 match line of the second pair of match lines.

1 16. (original) The CAM device of claim 1 wherein the first logic circuit comprises an
2 AND gate having a first input coupled to the first match line of the first pair of
3 match lines and a second input coupled to the first match line of the second pair of
4 match lines.

1 17. (original) The CAM device of claim 16 further comprising storage circuits coupled
2 to the first match lines to store the states of respective match signals thereon and to
3 output the stored states of the respective match signals to the first and second inputs
4 of the AND gate.

1 18. (currently amended) The CAM device of claim 1 further comprising:
2 a first pair of precharge circuits coupled respectively to the first match lines of the
3 first pair of match lines and to the second match line of the second pairs of
4 match lines; and
5 a second pair of precharge circuits coupled respectively to the second match lines of
6 the first pair of match lines and to the first match line of the second pairs of
7 match lines.

1 19. (currently amended) The CAM device of claim 18 further comprising circuitry to
2 assert a first precharge enable signal to enable the first pair of precharge circuits to

3 precharge the first match lines of the first pair of match lines and the second match
4 line of the second pair of match lines during a first interval, and to assert a second
5 precharge enable signal to enable the second pair of precharge circuits to precharge
6 the second match lines of the first pair of match lines and the first match line of the
7 second pair of match lines during a second interval.

1 20. (original) The CAM device of claim 19 wherein the CAM device further comprises
2 control circuitry to initiate a first compare operation in the first and second rows of
3 CAM cells during the first interval and to initiate a second compare operation in the
4 first and second rows of CAM cells during the second interval, the first compare
5 operation producing match results on the second pair of match lines and the second
6 compare operation producing match results on the first pair of match lines.

1 21. (original) A content addressable memory (CAM) device comprising:
2 a plurality of row pairs of CAM cells, wherein each row of CAM cells in a row pair
3 is coupled to a plurality of match lines; and
4 a plurality of logic circuits each having inputs coupled to the plurality of match
5 lines of a corresponding row pair of CAM cells, each of the plurality of logic
6 circuits configured to selectively combine match results on the plurality of
7 match lines of both rows of a corresponding row pair and output a composite
8 match signal.

1 22. (original) The CAM device of claim 21 wherein each CAM cell within each row of
2 CAM cells in a row pair includes a plurality of compare circuits coupled
3 respectively to the plurality of match lines.

1 23. (original) The CAM device of claim 22 wherein each CAM cell within each row of
2 CAM cells in a row pair includes a memory cell coupled to each of the plurality of
3 compare circuits within the CAM cell.

1 24. (original) The CAM device of claim 21 wherein each of the plurality of logic
2 circuits comprises a logic AND gate to logically AND the match results on a
3 respective pair of match lines of the plurality of match lines.

1 25. (original) A content addressable memory (CAM) device comprising:
2 a plurality of CAM cells each including a first compare circuit and a second
3 compare circuit;
4 a plurality of first match lines coupled to the first compare circuits included in the
5 plurality of CAM cells;
6 a plurality of second match lines coupled to the second compare circuits included in
7 the plurality of CAM cells; and
8 a plurality of logic circuits each coupled to a respective one of the first match lines
9 and a respective one of the second match lines, each logic circuit being
10 configured to output a match signal having a state according to the state of the
11 one of the first match lines and the state of the one of the second match lines.

1 26. (original) The CAM device of claim 25 wherein each of the plurality of logic
2 circuits is configured to output a match signal in a first state if the one of the first
3 match lines indicates a match and the one of the second match lines indicates a
4 match, each of the plurality of logic circuits being further configured to output a

5 match signal having a second state if either of the one of the first match lines and
6 the one of the second match lines indicates a mismatch.

1 27. (original) The CAM device of claim 26 wherein each of the plurality of logic
2 circuits comprises a logic AND gate having a first input coupled to the one of the
3 first match lines and a second input coupled to the one of the second match lines.

1 28. (original) The CAM device of claim 27 wherein each of the plurality of logic
2 circuits further comprises a select circuit having a first input coupled to an output of
3 the logic AND gate and a second input coupled to the one of the first match lines.

1 29. (original) The CAM device of claim 28 wherein the select circuit is a multiplexer.

1 30. (original) The CAM device of claim 25 further comprising a priority encoder
2 coupled to receive the match signals output by the plurality of logic circuits.

1 31. (original) A method of operation within a content addressable memory (CAM)
2 device, the method comprising:
3 simultaneously performing first and second compare operations in an array of CAM
4 cells to generate first and second sets of match signals; and
5 logically combining the first set of match signals with the second set of match
6 signals to generate a set of resultant match signals.

1 32. (original) The method of claim 31 wherein simultaneously performing first and
2 second compare operations in an array of CAM cells comprises simultaneously
3 providing first and second comparands to the array of CAM cells via first and

4 second compare ports, respectively.

1 33. (original) The method of claim 32 wherein the CAM cells in the array of CAM
2 cells are arranged in rows, each row of CAM cells being coupled to a corresponding
3 pair of match lines, and wherein simultaneously performing first and second
4 compare operations in the array of CAM cells further comprises receiving the first
5 and second comparands in each of the rows of CAM cells, each row of CAM cells
6 outputting a first match signal on a first match line of the corresponding pair of
7 match lines according to whether the first comparand matches a value stored within
8 the row of CAM cells, and each row of CAM cells outputting a second match signal
9 on a second match line of the corresponding pair of match lines according to
10 whether the second comparand matches the value stored within the row of CAM
11 cells.

1 34. (original) The method of claim 31 wherein simultaneously performing first and
2 second compare operations comprises simultaneously comparing a value stored
3 within each CAM cell of the CAM array with a portion of a first comparand value
4 and a portion of a second comparand value.

1 35. (original) The method of claim 31 wherein logically combining the first set of
2 match signals with the second set of match signals comprises combining each
3 match signal of the first set of match signals with a respective match signal of the
4 second set of match signals to generate a respective one of the resultant match
5 signals.

1 36. (original) The method of claim 35 wherein combining each match signal of the first
2 set of match signals with a respective match signal of the second set of match
3 signals comprises logically ANDing each match signal of the first set of match
4 signals with the respective match signal of the second set of match signals to
5 generate the respective one of the resultant match signals.

1 37. (original) The method of claim 31 further comprising selecting either the set of
2 resultant match signals or the first set of match signals to be output as a selected set
3 of match signals.

1 38. (original) The method of claim 37 further comprising generating a match address
2 based on the selected set of match signals.

1 39. (original) A content addressable memory (CAM) device comprising:
2 an array of CAM cells;
3 means for simultaneously performing first and second compare operations in the
4 array of CAM cells to generate first and second sets of match signals; and
5 means for logically combining the first set of match signals with the second set of
6 match signals to generate a set of resultant match signals.

1 40. (original) The CAM device of claim 39 wherein the means for simultaneously
2 performing first and second compare operations in the array of CAM cells
3 comprises means for simultaneously providing first and second comparands to the
4 array of CAM cells via first and second compare ports, respectively.

1 41. (original) The CAM device of claim 39 wherein the means for simultaneously
2 performing first and second compare operations comprises means for
3 simultaneously comparing a value stored within each CAM cell of the CAM array
4 with a portion of a first comparand value and a portion of a second comparand
5 value.

1 42. (original) The CAM device of claim 39 wherein the means for logically combining
2 the first set of match signals with the second set of match signals comprises means
3 for combining each match signal of the first set of match signals with a respective
4 match signal of the second set of match signals to generate a respective one of the
5 resultant match signals.

1 43. (original) The CAM device of claim 39 further comprising means for selecting
2 either the set of resultant match signals or the first set of match signals to be output
3 as a selected set of match signals.

1 44. (original) The CAM device of claim 43 further comprising means for generating a
2 match address based on the selected set of match signals.